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| **SESSION** | **February/MARCH 2024** |
| **PROGRAM** | **MASTER OF COMPUTER APPLICATIONS (mCA)** |
| **SEMESTER** | **I** |
| **course CODE & NAME** | **DCA6105 & Computer architecture** |
| **CREDITS** | **4** |
| **nUMBER OF ASSIGNMENTS & Marks** | **02**  **30** |

**Set-I**

**1. Differentiate between RISC and CISC.**

**Ans:**RISC (Reduced Instruction Set Computer) and CISC (Complex Instruction Set Computer) are two different computer architectures with distinct characteristics.

**Let's differentiate between them based on various factors:**

**1. Instruction Set Complexity:**

- RISC: RISC architectures have a reduced and simplified instruction set, typically consisting of simple instructions that perform basic operations.

- CISC: CISC architectures have a more complex instruction set, including instructions that can perform multiple operations or address various addressing modes in a single instruction.

**2. Instruction Length:**

- RISC: RISC instructions are generally of fixed length, making instruction decoding

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**2. What are addressing modes? Explain various addressing modes with example.**

**Ans:**Addressing modes are techniques used by a CPU to specify the operand's address in memory or register for an instruction. They define how the CPU interprets the operand's address and accesses data from memory or registers. Different addressing modes provide flexibility in accessing operands and optimize program execution.

**Here are some common addressing modes along with examples:**

**1. Immediate Addressing:**

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**3. What are pipelining hazards? Explain various hazards in detail.**

**Ans:**Pipelining hazards are situations that arise in pipelined processors, where the execution of instructions is hindered or delayed, leading to suboptimal performance. These hazards can occur due to various factors, including dependencies between instructions, pipeline structure, and resource constraints.

**There are three main types of hazards in pipelining:**

**1. Structural Hazards:**

- Structural hazards occur when the hardware resources required to execute multiple

**Set-II**

**4. Differentiate between unconditional and conditional branch.**

**Ans:Pipelining hazards** are situations that arise in pipelined processors, where the execution of instructions is hindered or delayed, leading to suboptimal performance. These hazards can occur due to various factors, including dependencies between instructions, pipeline structure, and resource constraints.

**There are three main types of hazards in pipelining:**

**1. \*\*Structural Hazards\*\*:**

- Structural hazards occur when the hardware resources required to execute multiple instructions simultaneously are not available.

**5. Describe in brief the architecture of vector processor. What are some of the key limitations of this architecture?**

**Ans:**A vector processor is a type of processor architecture designed to execute operations on vectors or arrays of data with a single instruction. It is optimized for performing parallel computations on large datasets, making it well-suited for tasks such as scientific simulations, image processing, and numerical computations.

**Here's a brief overview of the architecture of a vector processor:**

**1. \*\*Vector Registers\*\*:**

**-** Vector processors typically feature specialized vector registers capable of storing multiple data elements (e.g., floating-point numbers or integers) as a single vector.

**6. What do you understand by Parallel Processing? Also, explain Serial Processor and True Parallel Processor.**

**Ans:**Parallel processing refers to the simultaneous execution of multiple tasks or portions of a task using multiple processing units. In parallel processing, tasks are divided into smaller sub-tasks that can be executed independently and concurrently, leveraging multiple processors or processor cores to achieve higher performance and throughput.

**1. \*\*Serial Processor\*\*:**