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| **SESSION** | **February/MARCH 2024** |
| **PROGRAM** | **bachelor OF COMPUTER APPLICATIONS (bCA)** |
| **SEMESTER** | **2** |
| **course CODE & NAME** | **DCA1205** |
| **CREDITS** | **4** |

**Set-Ist**

**1. Explain the various Boolean laws with logic diagrams.**

**Ans:**

**Boolean algebra** is a branch of mathematics that deals with binary variables and logical operations. The basic laws of Boolean algebra are essential for simplifying and analyzing digital circuits. Below are the key Boolean laws along with their explanations and logic diagrams.

**1. \*\*Identity Law\*\***

- \*\*AND Identity Law:\*\* \( A \cdot 1 = A \)

- \*\*OR Identity Law: \*\* \( A + 0 = A \)

 **\*\*AND Identity Law:\*\***

```

 A ----|&|---- Output (A)

 | 1 |

 ```

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**2. Define the term logic gates. Explain the various basic gates with their symbols and truth table.**

**Ans:**
**Logic Gates:-**

**Logic gates** are the fundamental building blocks of digital circuits. They perform basic logical functions and are used to implement digital logic operations in computers, processors, and other digital systems. Each gate takes one or more binary inputs and produces a single binary output.

**Basic Logic Gates**

**1. \*\*AND Gate\*\***

 **- \*\*Symbol:\*\***

 ```

 A ----| & |---- Output (A AND B)

 | |

 B ----| |

 ```

 **- \*\*Truth Table: \*\***

 | A | B | A AND B |

 |---|---|---------|

 | 0 | 0 | 0 |

 | 0 | 1 | 0 |

 | 1 | 0 | 0 |

 | 1 | 1 | 1 |

**3. Explain the method of Karnaugh map simplification with don’t care condition. Give example.**

**Ans:**

**Karnaugh maps (K-maps)** are a graphical tool used to simplify Boolean expressions and minimize the number of logic gates needed in a digital circuit.

When simplifying expressions using K-maps, "don't care" conditions (denoted as X) are used to further reduce the complexity of the expression. These don't care conditions represent input combinations that do not affect the output and can be treated as either 0 or 1, depending on which helps in simplification.

**Steps for Simplifying**

**Using Karnaugh Map with Don’t Care Conditions Create the Karnaugh Map:**

**Set-IInd**

**4. Explain the working of JK flip flop?**

**Ans:**A JK flip-flop is a type of bistable multivibrator, an essential component in digital electronics used for storing binary data. It is an enhancement of the SR flip-flop (Set-Reset flip-flop) that eliminates the "invalid" state by ensuring that inputs J and K can never both be high simultaneously when the clock is triggered.

**JK Flip-Flop Overview Inputs:** J (Set input) K (Reset input) CLK (Clock input) Sometimes a Preset (PRE) and Clear (CLR) inputs for setting or resetting the flip-flop asynchronously.

**Outputs:** Q (Current state) Q' (Complement of the current state) Working Principle The state of the JK flip-flop changes at the clock's edge (usually the rising edge) based on the values of the J and K inputs.

**5. Explain the shift register in detail.**

**Ans:**

A shift register is a type of digital memory circuit used in computers and other devices to store and shift data. It consists of a series of flip-flops, each capable of storing one bit of data, and is used for data storage, data transfer, and data manipulation.

**Types of Shift Registers Shift registers can be classified based on the direction of data flow and the method of input and output.**

**The main types are:**

**Serial-In Serial-Out (SISO)**

**Parallel-In Parallel-Out (PIPO)**

Bidirectional Shift Register

**3. Parallel-In Serial-Out (PISO)**

**Shift Register**

In a PISO shift register, data is loaded in parallel and then shifted out serially.

**Working Principle:** Parallel data is loaded into the register simultaneously.

At each clock pulse, the data is shifted out serially.

**Diagram:**

Parallel Inputs --> [FF1] --> [FF2] --> [FF3] --> ... --> [FFn] --> Serial Output

 (D1, D2, D3, ..., Dn)

**4. Parallel-In Parallel-Out (PIPO)**

**Shift Register**

In a PIPO shift register, data is loaded and read out in parallel.

**Working Principle:**

**6. Discuss about the Master slave flip flop**

**Ans:**A master-slave flip-flop is a type of sequential logic circuit constructed from two separate flip-flops, referred to as the master flip-flop and the slave flip-flop. It is designed to address the problem of race conditions that can occur in certain types of flip-flops, particularly in edge-triggered designs.

**Working Principle** The master-slave flip-flop operates in two phases: the master phase and the slave phase. During each phase, one flip-flop is responsible for latching the input data, while the other flip-flop remains inactive.

**Master Phase:** During the master phase, the master flip-flop latches the input data based on the clock signal's rising edge. The input data is allowed to propagate through the master flip-flop's internal logic and is stabilized. Any changes to the input data during this phase do not affect the output.